SPECIFICATION

Please amend paragraph [0016] of the specification as follows.

[0016] FIG. 1 shows a processing unit 10 of the invention. Unit 10 is for example part of an EPIC processor to process multiple program threads through multiple pipelines 12. Pipelines 12 include an array of pipeline execution stages, known to those skilled in the art, to process instructions incrementally, such as in the fetch stage F, the register read stage R, the execute stage E, the detect exception stage D, and the write-back stage W. Thread controller 30 is illustratively shown with urgency indicators 32 that represent urgency of threads 15. For example, urgency indicator 32(1) indicates urgency of thread 15(1), urgency indicator 32(2) indicates urgency of thread 15(2) and urgency indicator 32(M) indicates urgency of thread 15(M). Unit 10 preferably has multiple instruction pointers 14(1), 14(2)...14(M) to accommodate processing multiple threads 15(1), 15(2)... [(]15(M) through units 12. A cache 13 buffers data from associated pipelines 12 to register files 16. The plurality of register files 16(1), 16(2)...16([N]M) provide per-cycle storage of data for unit 10, via bus 18; various architected states may be stored in register files 16(1), 16(2)...16([N]M), including write-back data from the W stage. Bypass logic 20 may be used to accommodate bypass and speculative data transfers to and between pipelines 12 and register file 16.